CLAIMS

What is claimed is:

1. A method for restoring CMOS parameter values in a computer having a power button, wherein the method comprises:

pressing the power button for a predetermined time delay while the computer is performing a power-on self test ("POST"), thereby placing the computer in an OFF state; and

momentarily pressing the power button to turn on the computer.

2. The method of claim 1, wherein the predetermined time delay is at least four seconds.

3. A method for restoring a CMOS memory to a backup condition in a computer having a power switch, wherein the method comprises:

closing the power switch for at least a predetermined time;

opening the power switch; and

momentarily closing the power switch for less than the predetermined time.

4. The method of claim 3, wherein said closing action is performed while the computer is performing a power-on self-test ("POST").

5. The method of claim 3, further comprising:

before said closing, momentarily closing the power switch to initiate a POST.

6. The method of claim 4, wherein said predetermined time is at least four seconds.

7. A method for setting CMOS parameter values in a computer equal to stored backup values, wherein the method comprises:

determining if a power-button-override bit has been set while a POST-in-progress bit was set; and

if so, copying stored backup values into memory locations of the CMOS parameters.

8. The method of claim 7, wherein the determining includes:

before setting the POST-in-progress bit, comparing the power-button-override bit to zero; and

if the power-button-override bit is not equal to zero, comparing the POST-in-progress bit to zero.

9. The method of claim 8, wherein the determining further includes:

if the POST-in-progress bit is not equal to zero, setting a CMOS-restore bit to one.

10. The method of claim 8, further comprising:

setting the POST-in-progress bit to one before performing a POST routine;

performing a POST routine; and

if the POST routine completes successfully, resetting the POST-in-progress bit to zero.

11. The method of claim 10, further comprising:

if the POST routine completes successfully, determining if any CMOS parameter values have been changed; and

if any CMOS parameter values have been changed, storing a backup copy of the CMOS parameter values.

12. A computer system which comprises:

a nonvolatile configuration memory configured to store computer configuration parameters;

a nonvolatile BIOS memory configured to store basic input/output system ("BIOS") software;

a CPU coupled to the nonvolatile configuration memory, wherein after a system reset signal is asserted the CPU is configured to initialize the computer using said BIOS software and said computer configuration parameters stored in the configuration memory; and

a power switch,

wherein said BIOS configures the CPU to determine if during a previous boot operation the power switch was closed for at least a predetermined time, and if so, configures the CPU to replace the computer configuration parameter values with backup parameter values.

13. The computer system of claim 12, wherein the predetermined time is four seconds.

14. The computer system of claim 12, wherein the BIOS further configures the CPU to store a backup copy of the computer configuration parameter values only if the CPU successfully completes a computer system power-on self-test ("POST") procedure.

15. The computer system of claim 12, wherein the BIOS further configures the CPU to backup the computer configuration parameter values only if the computer configuration parameter values have been changed and the CPU has successfully completed a computer system power-on self-test ("POST") procedure.

16. The computer system of claim 12, wherein the CPU determines that the power switch was closed for at least a predetermined time during a previous boot operation by determining before a POST procedure is initiated if both a post-in-progress bit and a power-button-override bit are asserted.